METHOD AND APPARATUS OF ZERO DEFLECTION

BACKGROUND

[001] In modern wireless communication systems such as cellular communication systems, radio transmitters in general and radio transmitters which may comprise a polar feedback loop, may transmit Radio Frequency (RF) signals at variable power levels. The RF signals may have a discontinuity in phase and may have variable amplitude. Zero crossing of the RF signal may cause discontinuity in phase. In order to enable the zero crossing of the signal the transmitter may need to incorporate wide dynamic range amplifier. The zero crossing may also cause degeneration of the transmitter Adjacent Channel Power Ratio (ACPR) which is out of most cellular standard limits.

[002] However, transmitters that enable to transmit RF signal which has phase zero crossing may involve the use of complicated circuitry that may increase the overall cost of the transmitter. In addition, transmitters that may comprise polar feedback loop may not be able to perform phase measurements in order to control the phase of the transmitter output signal. Thus, there is a continuing need for better ways of eliminating the phase zero crossing of the signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[003] The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

[004] Figs. 1A and 1B are block diagrams of a transmitter in accordance with some embodiments of the present invention;

[005] Fig. 2 is a flow chart diagram of a method of deflecting a signal in accordance with an embodiment of the present invention;

[006] Fig. 3 is an exemplary illustration of possible transitions of signals on an I/Q trajectory complex plane of a two code transmitter in accordance with some embodiments of the present invention; and

[007] Fig. 4 is a graph illustrating calculation of a deflection value in accordance with some embodiments of the present invention;

[008] It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[009] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

[0010] Some portions of the detailed description which follow are presented in terms of algorithms and symbolic representations of operations on data bits or binary digital signals within a computer memory. These algorithmic descriptions and representations may be the techniques used by those skilled in the data processing arts to convey the substance of their work to others skilled in the art.

[0011] In the following description and claims, the terms "chip", "PN code", and "zero crossing" along with their derivatives, may be used. It should be understood that these terms are not intent as synonyms for each other. The term "chip" may be used to describe multiple sub-bits in a direct sequence spread spectrum technique. The direct sequence spread spectrum technique is

a digital modulation technique in which a digital signal is spread over a wide frequency band so that it has a noise-like spectrum. This is done by breaking up each data bit into multiple sub-bits. Chips may also be referred to in this application as PN code bits (Pseudo Noise code bits). The term "zero crossing" may be used to describe transitions of an amplitude and a phase of a signal through a zero amplitude level.

[0012] Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as "processing", "computing", "calculating", "determining", "estimating" or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities within the computing system's registers and/or memories into other data similarly represented as physical quantities within the computing system's memories registers or other such information storage, transmission or display devices.

[0013] It should be understood that the present invention may be used in a variety of applications. Although the present invention is not limited in this respect, the circuits and techniques disclosed herein may be used in many apparatuses such as transmitters of a radio system. Transmitters intended to be included within the scope of the present invention include, by a way of example only, cellular radiotelephone transmitters, two-way radio transmitters, digital system transmitters, analog system transmitters and the like.

[0014] Types of cellular radiotelephone transmitters intended to be within the scope of the present invention include, although not limited to, Code Division Multiple Access (CDMA) and wide band CDMA (W-CDMA) cellular radiotelephone transmitters for transmitting spread spectrum signals. Time Division Multiple Access (TDMA) transmitters, Extended-TDMA (E-TDMA) transmitters with a non-constant envelop digital modulation techniques, and the like.

[0015] Turning to Figs. 1A and 1B, a transmitter 100 in accordance with an embodiment of the invention is shown. The transmitter 100 includes a data source 105, a baseband block 190, an amplifier 170 and an antenna 180. The baseband block 190 may be a hardware device or may be implemented in software by a computer. An example of the baseband block 190 is a general computer which received signals from the data source 105, process the signals and output the processed signals to the amplifier 170 or a digital signal processor (DSP) for doing the same. The baseband block 190 may comprise a channelization and spreading block 110, a pulse shaping filter 120, an estimator 130, a deflector 135, a digital to analog (D/A) converter 140, a reconstruction filter 150, and an upconverter 160.

[0016] An example of the operation of transmitter 100 will be described now. In this particular example, transmitter 100 may be adapted to transmit spread spectrum signal that may include the data structure of a W-CDMA system or a CDMA system or a CDMA 2000 system or the data structure of another spread spectrum system. However, in alternative embodiments of the invention, transmitter 100 may be adapted to transmit other types of cellular radiotelephone signals such as described above.

[0017] In operation, the data source 105 outputs an In Phase/Quadrature (I/Q) data stream that includes data symbols which include blocks of bits to the baseband block 190. Inside the baseband block 190, the channelization and spreading block 110 may be channelized and spread with a spreading technique that uses basic complex scrambling and Pseudo-Noise (PN) signals the data symbols for providing an In-Phase (I) signal and a Quadrature (Q) signal.

[0018] In third generation (3G) cellular systems for example, W-CDMA, spreading technique such as Hybrid Phase Shift Keying (HPSK) which may also be known to the person skilled in the art as Orthogonal Complex Quadrature Phase Shift Keying (OCQPSK) may be used. However, other spreading techniques, for example, Offset Quadrature Phase shift Keying (OQPSK) and alike may be used. The output of the channelization and spreading module 110

are I and Q signals which may comprise PN code bits. The PN code bits are also known to those skilled in the art of spread spectrum systems as chips.

[0019] Although, the scope of the invention is not limited in this respect, in one embodiment of the invention, the I portion of the chips and the Q portion of the chips may be input to the pulse shaping filter 120. The pulse shaping filter 120 may include a first filter to shape the I portion of the chips and a second filter to shape the Q portion of the chips.

[0020] Although, the scope of the invention is not limited in this respect, the I portion of the chips and the Q portion of the chips may be input to the estimator 130. Although, it should be understood that the scope and application of the present invention is in no way limited to these examples, the pulse shaping filter 120 may include a low pass filter. The low pass filter may limit the signal spectrum and may prevent an inter symbol interference. The output from the shaping filter 120 may be I/Q samples at double chip rate or higher. The I/Q samples may be input to estimator 130 and to the deflector 135.

[0021] Although, the scope of the invention is not limited in this respect, in other embodiments of the invention, the estimator 130 may receive at least two consecutive chips $C_{(n)}$ and $C_{(n+1)}$ and at least two consecutive samples $S_{(n)}$ and $S_{(n+1)}$. The samples $S_{(n)}$ and $S_{(n+1)}$ may be sampled at each chip interval. The estimator 130 is adapted to predict an occurrence of a predetermined amplitude level in an in-phase and a quadrature phase (I/Q) complex trajectory. The estimator 130 may use this prediction to determine if zero crossing of the trajectory complex plane may be possible.

[0022] For candidate signals of zero crossing, the estimator 130 outputs to the deflector 135 corrective parameters according to at least two consecutive blocks of bits (chips). The estimator 130 may be adapted to provide the trajectory corrective parameters according to the estimated distance between the origin of the complex trajectory plane to the I/Q complex trajectory.

[0023] Although, the scope of the invention is not limited in this respect, the data of trajectory corrective parameters may be adjusted according to adjustable deflection window. The deflection window may be any type of a

weighting window. Although it is not limited to this example, the adjustable deflection window may be a Kaiser window . However, other types of windows such as a Bartlett window, Blackman window, Chebyshev window, Hamming window or Hanning window may be used.

[0024] The deflector 135 deflects the signals from the origin of the complex trajectory plane according to the estimator prediction by adding trajectory corrective parameters to the samples surrounding samples $S_{(n)}$ and $S_{(n+1)}$. In another embodiment of the present invention which is illustrated in Fig. 1B, a sampler 115 may be added to receive chips $C_{(n)}$ and $C_{(n+1)}$ to provide samples $S_{(n)}$ and $S_{(n+1)}$ of I and Q to the estimator 130. Therefore in this embodiment, the estimator 130 may not receive I and Q signals from the output of the shaping filter 120.

[0025] The I and Q signals from the deflector 135 may be input to D/A 140. As shown, the D/A 140 may convert the data of the I and Q signals into I and Q analog signals. The I and Q analog signals may be input to the reconstruction filter 150. The reconstruction filter 150, may include for example, a low pass filter that filters harmonic distortion from the I analog signal and a low pass filter that filters harmonic distortion from the Q analog signal. Furthermore, the reconstruction filter 150 may filter a distortion of signal replication that may have been created as a result of the sampling rate by the sampler 115, from the I and Q analog signals. In other embodiments of the invention, the reconstruction filter 150 may be replaced by other types of filters or may not be needed in the case of a sampling rate which may not result in a signal replication.

[0026] The I and Q analog signals may be input to the upconverter 160. As shown, the upconverter 160 combines the I and Q analog signals and up converts the combined signal into a radio frequency (RF) signal. The amplifier 170 amplifies the RF signal and outputs the amplified RF signal to antenna 180. The antenna 180 may be adapted to the frequency of the RF signal and transmit the amplified RF signal.

[0027] Although, the scope of the present invention is not limited to the above described embodiments of the invention, the modules channelization and

spreading 110, shaping filter 120, D/A 140, reconstruction filter 150, upconverter 160 and the amplifier 170 may be standard modules which may be used in spread spectrum transmitters such as CDMA, W-CDMA or CDMA 2000. However, other known implementations which may be known to persons skilled in the art, may be used. For example, the amplifier 170 may include an outphasing amplifier with a reactive termination.

[0028] Although embodiments of the present invention are not limited in this respect, the method for deflecting signal which is a candidate for zero crossing will be described now with references to Figs. 2, 3 and 4.

[0029] Turning now to Fig. 2, a flow chart of a method of deflecting a signal from the origin of the complex plane is described. The method starts with testing two consecutive chips $C_{(n)}$ and $C_{(n+1)}$ for zero crossing possibility, as is shown in block 200. Testing of zero crossing possibility may be based on a prior knowledge of the type of the transmitter and of the type of modulation.

[0030] Fig. 3 is an example of possible transitions of signals on an I/Q trajectory complex plane of a two-code transmitter. For a two-code transmitter only 3 of 8 possible transitions may be candidates for zero crossing. As is shown in Fig. 3, vectors 301, 302, 303, 304, 305,. 306, 307 and 308 are the possible transitions. Transitions 304, 305 and 306 may be candidates for zero crossing. The dotted circle 310 shows a zone of possible zero crossing. The information of the transition may be processed from Dedicated Physical Data Channel (DPDCH) and Dedicated Physical Control Channel (DPCCH) bits of the chips $C_{(n)}$ and $C_{(n+1)}$.

[0031] Turning back to Fig. 2, the method proceeds with testing if zero crossing is possible for at least one of the 3 possible transitions, as is shown in 220. If none of the possible transitions is a candidate for zero crossing, then the next pair of chips $C_{(n+1)}$ and $C_{(n+2)}$ may be processed, as is shown at block 230. If candidate transitions for zero crossing are found, then the following algorithm for calculating trajectory minimum magnitude point (S_{min}) by using at least two consecutive data samples $S_{(n)}$ and $S_{(n+1)}$ of the elected signal may be used, as is

shown at 240. The samples $S_{(n)}$ and $S_{(n+1)}$ are obtained at the chips $C_{(n)}$ and $C_{(n+1)}$ and may be dependent on the sampling rate R,

wherein $R = \frac{Samples}{Chips}$.

[0032] It should be understood that other methods for calculating the trajectory minimum magnitude may be used.

[0033] The method for calculating trajectory minimum magnitude S_{min} will be described with reference to Fig. 4. Fig. 4 shows the deflection of an elected signal 403 on an I/Q complex trajectory plane 400. FIG. 4 further shows a complex trajectory curve of the signal 402, a deflected signal (dotted curve) 405, a zero zone 401 and a zero zone radius R_0. Although it is not limited in this respect, a prior knowledge of the minimum point of the trajectory allows to define the level and the direction of shifting the elected signal 403 from the zero zone 401 of the IQ complex trajectory plane 400. The calculation of S_{min} may be based on S(R*n) and S(R*n+1) filtered samples of chip $C_{(n)}$. The drawing shows a part of IQ trajectory and S(4*n), S(4*n+1) and S_{min} points. For the sake of simplicity S(R*n), S(R*n+1) are called S1 and S2 respectively. An example of S1 and S2 is shown with Fig. 4.

[0034] Although the invention is not limited to the below formulae, an example of a linear estimation of the distance between the trajectory and the origin of the I/Q complex plane 400 will be described below. In this example,

(1) $S_\Delta = S_1 - S_2$,

is the difference vector between S_1 and S_2.

The linear estimation of the minimum trajectory point S_{min} may be calculated by equation (2)

(2) $$S_{min} = S_1 - S_\Delta \cdot \frac{I_1 \cdot I_\Delta + Q_1 \cdot Q_\Delta}{I_\Delta^2 + Q_\Delta^2}$$

The magnitude of S_{min} is used to calculate the magnitude of the shift 406 that should be applied to the trajectory.

(3) $R_{min} = |S_{min}| = \sqrt{I_{min}^2 + Q_{min}^2}$

[0035] An alternative equation to equation (3) may be an approximated formula for S_{min} magnitude calculation as shown below.

$$Rmin \cong |S_{min}| = |I_{min}| + \frac{|Q_{min}|}{2} - \frac{|Q_{min}|}{8} \quad I_{min} \geq Q_{min}$$

(4)

$$Rmin \cong |S_{min}| = |Q_{min}| + \frac{|I_{min}|}{2} - \frac{|I_{min}|}{8} \quad Q_{min} \geq I_{min}$$

[0036] The approximation (3) may introduce an error up to about 6.5%.

[0037] In some embodiments of the invention, the flowing method of obtaining test samples $S_{(n)}$ and $S_{(n+1)}$ may be used. In general, two or more test samples $S_{(n)}$, $S_{(n+1)}$, $S_{(n+2)}$ ... may not coincide with the samples of pulse shaping filter 120. In order to obtain additional samples at arbitrary times offset from the chips, a filter that includes the same filter shape of pulse shaping filter 120 and the sampling rate of Half-Nyquist rate (equal to chip rate) may be used. The samples of such a filter are chosen at a desired time offset from its center providing the same offset of the output samples on the signal's trajectory. The Half-Nyquist rate filter may yield one test sample at a predefined time offset from the chip $C_{(n)}$.

[0038] Although the scope of the invention is not limited in this respect, an example of a method for providing the above described filter with the receiving chips will be described now. Let us formally define Half-Nyquist rate filter and the filtering of the chips. Assume that the continuous impulse response of the filter is Fn(t), then the sampled filter response is: Fsn(n)=Fn(n/Rc+Toffset) where Rc is the chip rate and Toffset is the sampling offset.

[0039] Obtaining the test sample S_n associated with chip $C_{(n)}$ is done by convolving sequence of chips with the filter

$S_n = C'$:

$$S_n = C \oplus Fs_\delta = \sum_{i=-N}^{N} C(i+n) \cdot Fs_\delta(i),$$

where N is the length of the filter in the chips.

[0040] Turning back to Fig. 2, if $|S_{\min}|$ falls in the zero zone 401 (step 250) deflection of the trajectory is to be performed. Although the scope of the invention is not limited to this example, a soft deflection window may be added to IQ samples surrounding samples S(R*n), S(R*n+1), as is shown in 260. The deflection window may be centered around sample S(R*n). The length of the window may include 7 samples (2 chip duration). The samples of the window may be calculated by using, for example, base Kaiser window. However, other windows such as Rectangle, Triangle, Hanning, Hamming, Blackman, Lanczos, Tukey and the like may be used. An example of the window samples may be samples w = [w_{-3}, w_{-2}, w_{-1}, w_{-0}, w_1, w_2, w_3] and complex scaling factor – SC_{FACT}. The deflection window W which is used with the above example may be a complex sample sequence.

[0041] The deflection window may also be described by the following equations:

(5) $W(i,q) = SC_{FACT}(i,q) \cdot w$

scaling of the unity scalar window to the actual values for I and Q, wherein SC_{FACT} can be calculated using $|S_{min}|$, S_{min} and R_0 as it is shown in equation (6).

(6) $$SC_{FACT} = S_{\min} \cdot \left(\frac{R_0}{|S_{\min}|} - 1 \right)$$

[0042] However, the window scaling calculation may be done by using a look up table (LUT) as is shown by equation (7),

(7) $$SC_{FACT} = S_{dir} \cdot LUT\ (round\ |S_{\min}|),$$

wherein round, rounds the value of S_{min} into an integer value, and S_{dir} rotates vector S by +90° or -90°.

[0043] The rotation direction may be chosen so that signs of real and imaginary parts of S_{dir} become the same as signs of S_{min}. In other words, the direction of the trajectory shift may be normal to the trajectory and may not point to the origin. If we define $S_{dir}=I_{dir}+jQ_{dir}$ and $S=I+jQ$, then

$$(8)\quad \begin{aligned} I_{dir} &= |Q_{\Delta}| \cdot sign(I_{\min}) \\ Q_{dir} &= |I_{\Delta}| \cdot sign(Q_{\min}) \end{aligned}$$ - finding the direction vector of scaling window

[0044] The final step is deflecting the trajectory as is shown by equation (9).

$$(9)\quad S_{final}(m) = S(K+m) + W(m)$$

wherein K is the offset from the beginning of the processed data signal and m is the offset from the beginning of the window.

[0045] While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

[0046] What is claimed is: